coercive voltage is applied to the memory cell before the data is read from a selected memory cell into which the data "1" or "0" is written. On the other hand, in the fourth embodiment, the data "1" is first written into all of the memory cells in the cell array, and an electric potential differences which have the direction of the electric field directed from the plate line to the bit line so as to weaken the polarization, and which are smaller than the absolute value of the coercive voltage, are applied to these memory cells.

Next, the operation of the memory shown in FIG. 12 will be described with reference to a timing chart of FIGS. 13A to 13I.

A control signal ~~PLENABL~~ PLENBLE rises from "L" to "H" (VDD) and a preparation for driving the plate line is carried out as shown in FIG. 13B. After the control signal ~~PLENABL~~ PLENBLE rises to "H", the control signal PLON once rises to "H" in order to drive the plate line as shown in FIG. 13D. Because the equalizing control line EQL is set to "H" (VDD) as shown in FIG. 13A, NMOS transistors 17, 18, and 19 in the bit line equalizing/pre-charging circuit 11 shown in FIG. 4 are turned on, and all of the bit lines are equalized to 0V (GND) as shown in FIG. 13C.

Next, the control signal PLON falls to "L", and the control signal /TestPL falls to "L" as shown in FIGS. 13D and 13E. Further, due to row addresses being